Electric: a Multithreaded Integrated-Circuit Design System

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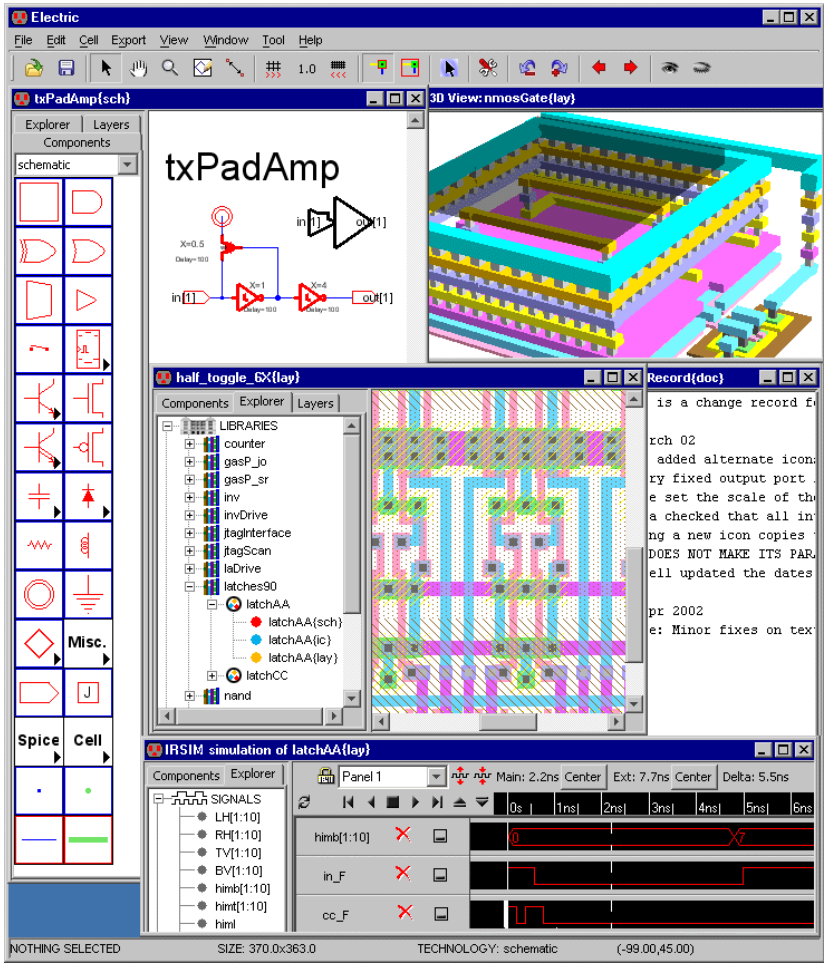
Sun Microsystems

and

Static Free Software



What is Electric?

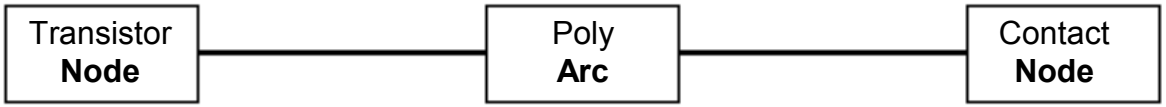
- **Complete integrated-circuit / schematics design system**
- **25 years old (first published in 1983)**
- **Originally written in C, translated to Java in 2003**
- **Open-source, used at universities, small businesses, etc.**

Electric's Circuitry Model

- **Schematic capture systems use connectivity model**
- **Integrated circuit systems use paint model**
- **Electric uses connectivity for schematics and ICs**

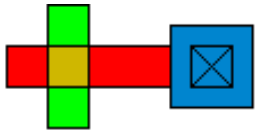
Circuitry as Nodes and Arcs

Transistor **Node** | Poly **Arc** | Contact **Node**

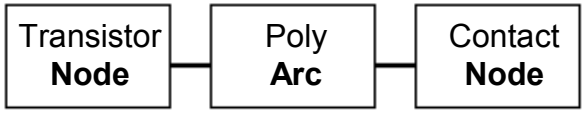


Hierarchy Implemented with Nodes

"Gate" Layout

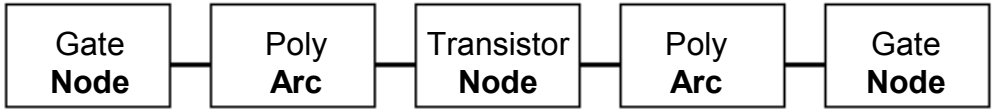


Representation



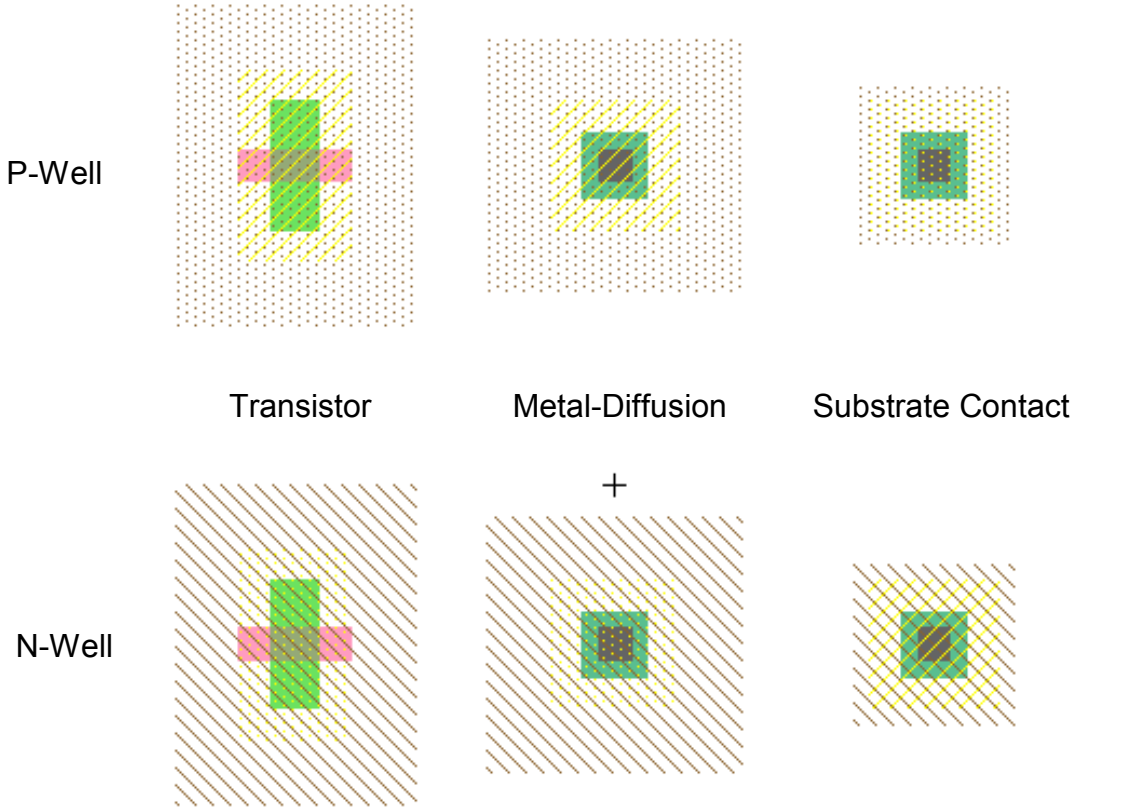
"TwoGate" Layout

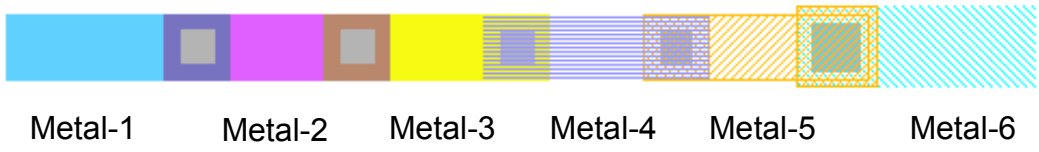
Representation



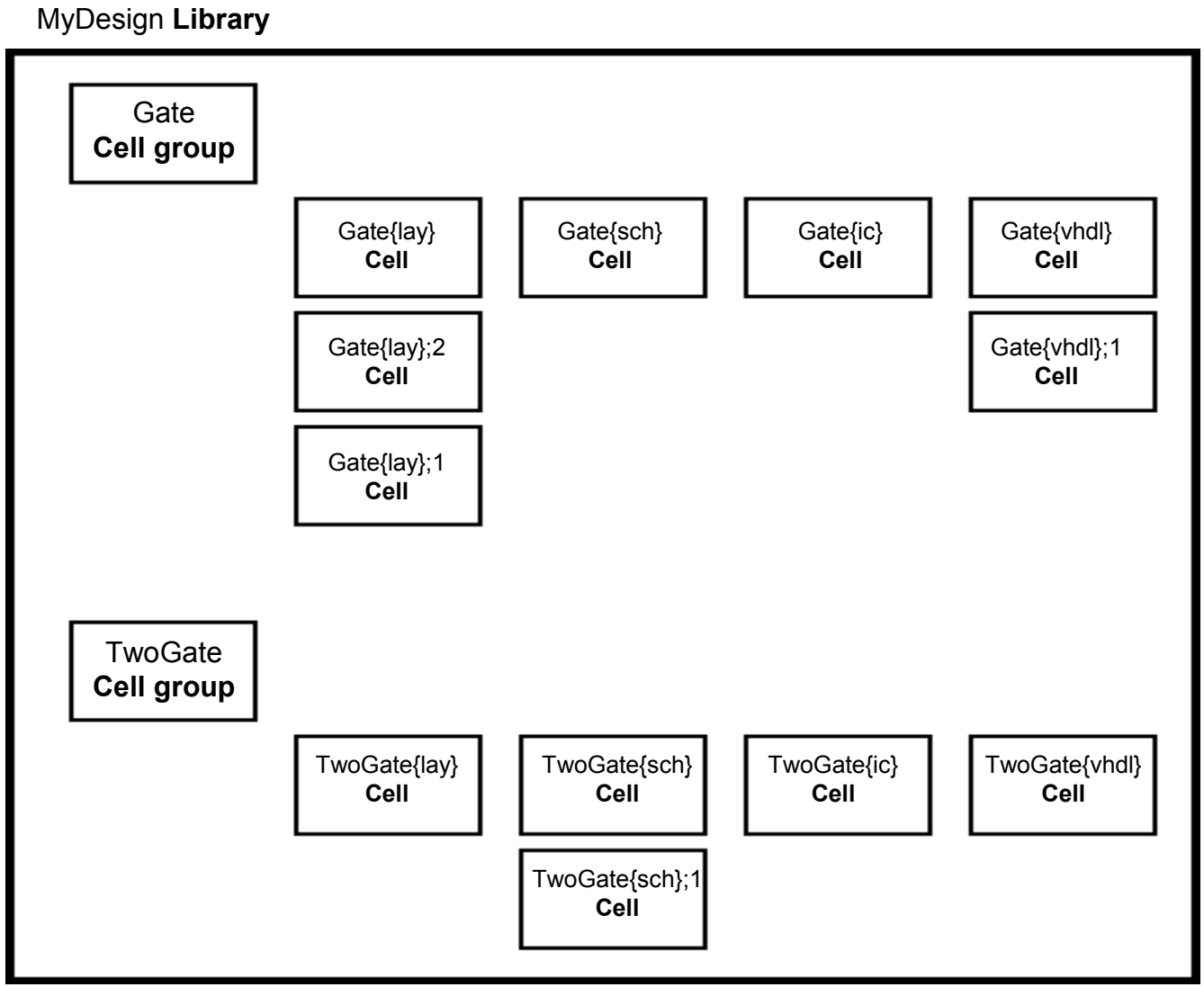
Flattened Layout

Primitive Components of CMOS





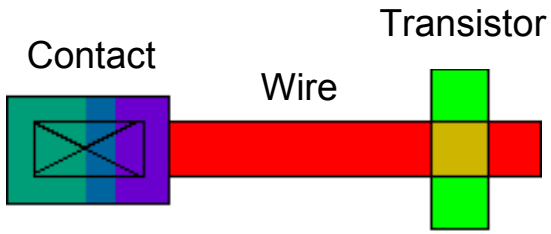
Hierarchy of Cells

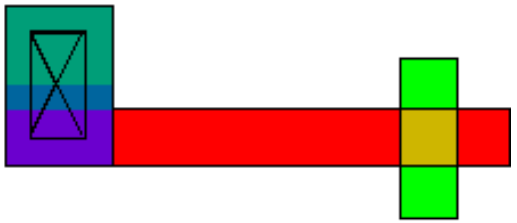


Electric Constraints

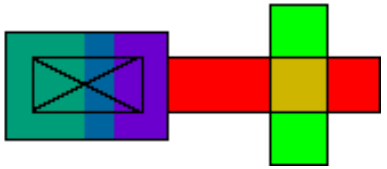
- **Holds layout together sensibly**
- **Works hierarchically**

Constraint System: Fixed-Angle Wires



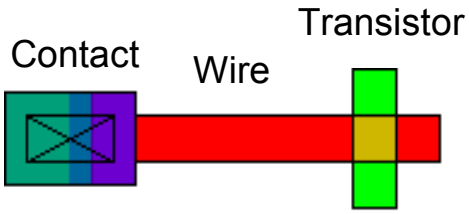


Contact rotated, fixed-angle wire



Contact moved right, fixed-angle wire

Constraint System: Rigid Wires

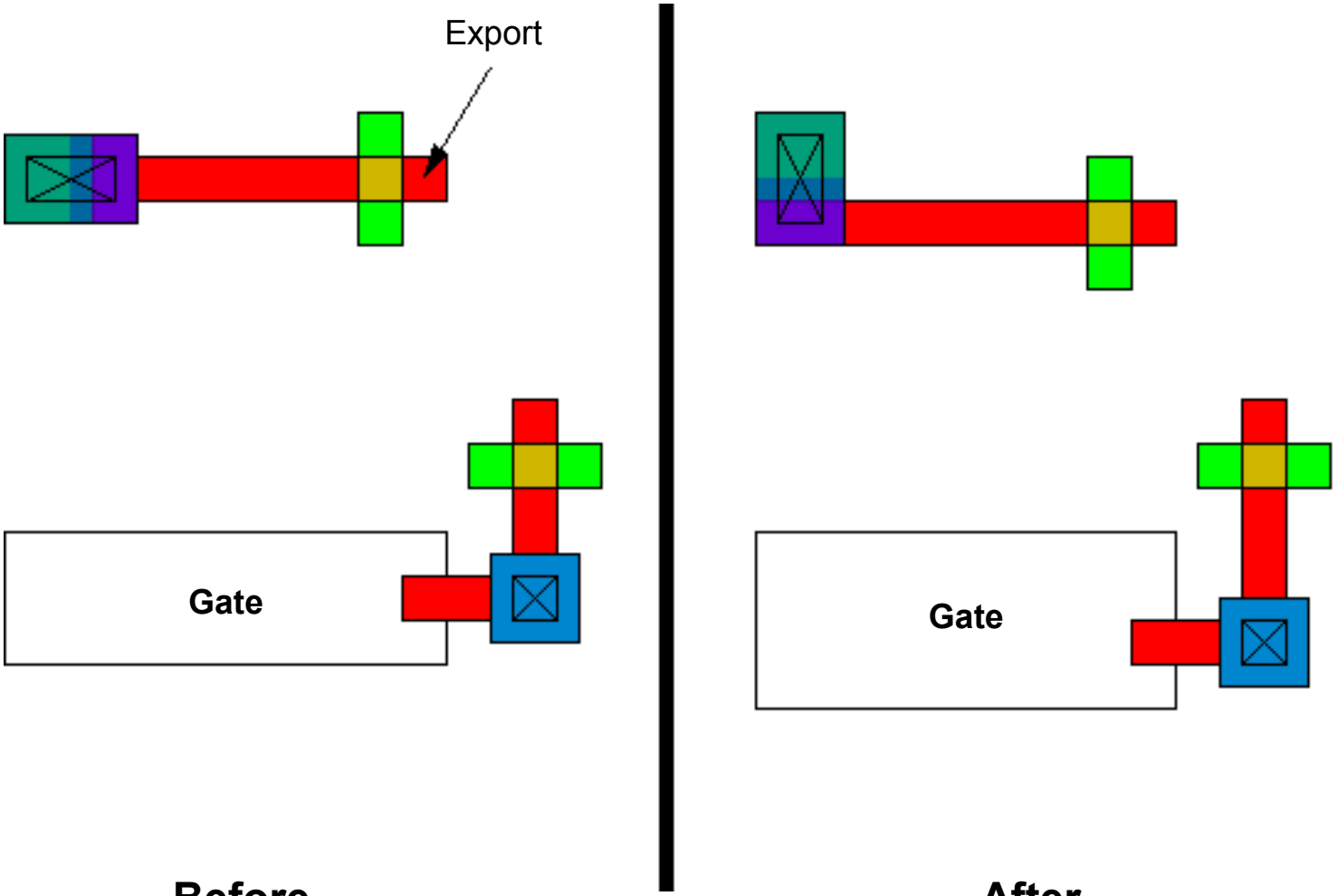


Contact rotated, unconstrained wire

Contact rotated, rigid wire

Contact moved right, rigid wire

Constraint System: Outward Propagation



Multithreading in Electric

- Simple translation to Java does not enable multithreading
  - Database is not thread-safe

- Creating thread-safe database
  - “Snapshot” of database is immutable
  - Multiple snapshots share most data
  - Database server manages snapshots
  - Client process manages the user interface

Multithreading DRC

- Design-rule checker uses multiple threads
- Each thread checks a different set of rules (poly, metal-1)
- Performance is improved 1.5X on 4-processor machine

Multithreading Routing

- Router creates wires on different metal layers
- Speedup 1: route multiple wires in parallel
  - Each router works in a nonintersecting area of the chip
- Speedup 2: route each wire twice
  - One processor does head-to-tail, other does tail-to-head
  - Fastest route cancels other processor
- Performance is improved 4X on 8-processor machine

Multithreading Well-Check

- Well check must analyze all well polygons on chip
  - Follows intersections to establish connectivity
- Multiple processors can aggregate connectivity
  - Conflicts (when two processors hit the same polygon)
- Performance improvement is linear or better!
  - In one cell, 6X speedup on 4-processor machine

Summary

- Powerful design system uses connectivity for IC design
- Constraint make design even more powerful
- Immutable database and Java code enables multithreading
- Multithreading experiments are under way

Further Reading

- **First published in 1983**

  Rubin, Steven M., "An Integrated Aid for Top-Down Electrical Design", Proceedings, VLSI '83 (Anceau and Aas, eds.), North Holland, Amsterdam, 1983.

- **Textbook in "Mead&Conway" VLSI System Series**

  Rubin, Steven M., *Computer Aids for VLSI Design*, Addison-Wesley, Reading, Massachusetts, 1987.

- **Overview in IEEE Communications**

  Rubin, Steven M., "A General-Purpose Framework for CAD Algorithms", IEEE Communications, Special Issue on Communications and VLSI, May 1991.

- **Upcoming DAC poster**

  Rubin, Steven M. and Garreton, Gilda, "Three-dimensional Visualization of Integrated Circuits in the Electric VLSI Design System", Proceedings 46th Design Automation Conference, July 2009.

- **User's Manual and Javadoc Internals**